

## **CLAIMS**

We claim:

- 1 1. A semiconductor package comprising:  
2 a substrate having a surface, said surface having a central region and an outer  
3 region;  
4 a first plurality of electrical connections on said outer region spaced apart by a  
5 first distance; and,  
6 a second plurality of electrical connections on said central region spaced apart by  
7 a second distance, wherein said second distance is smaller than said first distance.
- 1 2. The package of claim 1 wherein said first and second plurality of electrical  
2 connections are selected from the group comprising: input/output connections, power  
3 connections, and ground connections.
- 1 3. The package of claim 1 wherein said first and second plurality of electrical  
2 connections comprise an array of electrically conductive bumps.
- 1 4. The package of claim 1 wherein said first and second plurality of electrical  
2 connections comprise conductive lands.
- 1 5. The package of claim 1 further comprising a plurality of routing channels  
2 extending from said first and second plurality of electrical connections, wherein said

3 second electrical connections have more routing channels extending therefrom than  
4 said first electrical connections.

1 6. The package of claim 5 wherein said first plurality of electrical connections are  
2 spaced apart to allow at least four routing channels to pass between said first plurality of  
3 electrical connections, and said second plurality of electrical connections do not have a  
4 routing channel between said second plurality of electrical connections.

1 7. The package of claim 1 wherein said first and second electrical connections are  
2 positioned on said surface in a progressive pitch layout.

1 8. An integrated circuit comprising:  
2 an integrated circuit die having a surface, said surface having a central region  
3 and an outer region;  
4 a first plurality of leads on said outer region spaced apart by a first distance; and,  
5 a second plurality of leads on said central region spaced apart by a second  
6 distance, wherein said second distance is smaller than said first distance.

1 9. The integrated circuit of claim 8 wherein said first and second plurality of  
2 electrical connections are selected from the group comprising: input/output connections,  
3 power connections, and ground connections.

1 10. The integrated circuit of claim 8 wherein said first and second plurality of  
2 electrical connections comprise an array of electrically conductive bumps.

1 11. The integrated circuit of claim 8 wherein said first and second plurality of  
2 electrical connections comprise conductive lands.

1 12. The integrated circuit of claim 8 further comprising a plurality of routing channels  
2 extending from said first and second plurality of electrical connections, wherein said  
3 second electrical connections have more routing channels extending therefrom than  
4 said first electrical connections.

1 13. The integrated circuit of claim 12 wherein said first plurality of electrical  
2 connections are spaced apart to allow at least four routing channels to pass between  
3 said first plurality of electrical connections, and said second plurality of electrical  
4 connections do not have a routing channel between said second plurality of electrical  
5 connections.

1 14. The integrated circuit of claim 8 wherein said first and second electrical  
2 connections are positioned on said surface in a progressive pitch layout.

1 15. A printed circuit board comprising:  
2 a substrate having a surface, said surface having a central region and an outer  
3 region;  
4 a first plurality of electrical connections on said outer region spaced apart by a  
5 first distance; and,

6 a second plurality of electrical connections on said central region spaced apart by  
7 a second distance, wherein said second distance is smaller than said first distance.

1 16. The printed circuit board of claim 15 wherein said first and second plurality of  
2 electrical connections are selected from the group comprising: input/output connections,  
3 power connections, and ground connections.

1 17. The printed circuit board of claim 15 wherein said first and second plurality of  
2 electrical connections comprise an array of electrically conductive bumps.

1 18. The printed circuit board of claim 15 wherein said first and second plurality of  
2 electrical connections comprise conductive lands.

1 19. The printed circuit board of claim 15 wherein said first and second plurality of  
2 electrical connections comprise connector pins.

1 20. The printed circuit board of claim 15 further comprising a plurality of routing  
2 channels extending from said first and second plurality of electrical connections,  
3 wherein said second electrical connections have more routing channels extending  
4 therefrom than said first electrical connections.

1 21. The printed circuit board of claim 20 wherein said first plurality of electrical  
2 connections are spaced apart to allow at least four routing channels to pass between  
3 said first plurality of electrical connections, and said second plurality of electrical

4 connections do not have a routing channel between said second plurality of electrical  
5 connections.

1 22. The printed circuit board of claim 15 wherein said first and second electrical  
2 connections are positioned on said surface in a progressive pitch layout.

1 23. An apparatus comprising:

2 a substrate having a surface, said surface having a central region and an outer  
3 region;

4 a first plurality of electrical connections on said outer region spaced apart by a  
5 first distance; and,

6 a second plurality of electrical connections on said central region spaced apart by  
7 a second distance, wherein said second distance is smaller than said first distance.

1 24. The apparatus of claim 23 wherein said first and second plurality of electrical  
2 connections are selected from the group comprising: input/output connections, power  
3 connections, and ground connections.

1 25. The apparatus of claim 23 further comprising a plurality of routing channels  
2 extending from said first and second plurality of electrical connections, wherein said  
3 second electrical connections have more routing channels extending therefrom than  
4 said first electrical connections.

1 26. The apparatus of claim 25 wherein said first plurality of electrical connections are  
2 spaced apart to allow at least four routing channels to pass between said first plurality of  
3 electrical connections, and said second plurality of electrical connections do not have a  
4 routing channel between said second plurality of electrical connections.

1 27. The apparatus of claim 23 wherein said first and second electrical connections  
2 are positioned on said surface in a progressive pitch layout.